REMARKS

Claims 45, 46, 49-52, 54-57, 59, 60 and 68-76 are pending in this application.

Claims 72 and 76 stand rejected under 35 U.S.C. § 112, first paragraph, as the specification "described the 'first' and 'second' dielectric materials 24 and 34 as being the same, specifically, silicon dioxide." (Office Action at 2). The Office Action points out Figure 8 and pages 9-10 of the Specification, and on this basis, asserts that claims 72 and 76 "would be new matter." (Office Action at 2).

The Applicant disagrees. In the "Summary" part of the application, it is mentioned that "[A]fter the ions are implanted . . . the remainder of the trench can be filled with the same or another dielectric material." (Application at 3, lines 19-21). In addition, the partial filling of the trench with a dielectric material "can include growing an oxide layer such as silicon dioxide or depositing an insulating material using chemical vapor deposition or a combination of thermal growth and chemical vapor deposition." (Application at 3, lines 30-32; at 4, lines 1-2). Further, in the "Detailed Description" part of the application, it is clearly stated that "[S]uitable dielectric materials include oxides such as silicon oxide (SiO_2)," which can be either thermally grown or deposited by CVD. (Application at 6, lines 22-29). Thus, the present invention is not limited to the use of silicon oxide as the material for the first and second dielectrics, and a variety of other "suitable" dielectric materials could be used also. Moreover, the first and second dielectric materials may be the same or different. Accordingly, the subject matter of claims 72 and 76 is disclosed in the specification and it is not new matter.

Claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76 stand rejected under 35 U.S.C. § 103 as being unpatentable over Schuegraf et al. (U.S. Patent No. 5, 702, 976) ("Schuegraf") in view of Jeng (U.S. Patent No. 5, 492, 853) ("Jeng `853"). The Office Action asserts that the claimed first dielectric material reads on dielectric film 24 of Figure

3D of Schuegraf and that the claimed second dielectric material reads on dielectric material 26 of the same Figure. (Office Action at 3). The claimed "ions" also "read on subportions of a doped substrate 10 under trench dielectric 24." (Office Action at 3). Thus, as stated in the Office Action, the claimed ions do not distinguish over the ions in a doped substrate 10. (Office Action at 3).

The rejection is traversed. Schuegraf discloses trenches which are "refilled with a dielectric material" with low dielectric constant. (Col. 3, lines 61-62). However, none of these trenches have a first and a second areas which are filled with corresponding dielectric materials, as independent claim 68 of the present invention recites. Moreover, Schuegraf does not teach or suggest an ion implanted region directly below the second dielectric area. Schuegraf is also silent about any ions from said ion implanted region "being displaced away from said separated active regions," as independent claim 68 recites. In fact, Schuegraf does not even mention the existence of active regions in the "Detailed Description" or illustrate any such active regions in the "Drawings." Schuegraf is further silent about ions which are "displaced away from said active regions by a distance at least equal to a sidewall thickness of said first area filled with said first dielectric material," as independent claim 73 recites. Schuegraf does not have any discussion of ion implantation below a trench, much less of the recited spacing of the implanted regions.

The Examiner's reliance upon Jeng `853 is misplaced. Jeng `853 does not disclose either a trench isolation structure with "a first area filled with a first dielectric material . . . and a second area filled with a second dielectric material" or ion implantation directly below the second area with substantially all ions displaced away from active regions. Jeng `853 discloses only a trench having an oxide layer 54 (Figure 6) located at the bottom of the trench and a conductive layer 60 (Figure 6) in direct contact with the oxide layer 54. Thus, there is no teaching or suggestion in either of these two references, either

independently or combined, for the subject matter of claims 45, 46, 49-52, 54-57, 59, 60, 68-70, 72-74 and 76.

Claims 45, 46, 49-52, 54-57, 59, 60, 68-71, and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by either Jeng (U.S. Patent No. 5, 706, 164) ("Jeng `164") or Narita (U.S. Patent No. 5, 859, 451). With respect to Figure 12 of Jeng `164, the Office Action asserts that the claimed first and second dielectric materials read on subpotions of dielectric layer 7 and that the claimed ions read on subportions of P type substrate 1 under dielectric layer 7. (Office Action at 3). With respect to Figure 1 of Narita, the Office Action notes that the claimed first and second dielectric materials read on subportions of the field oxide 14. (Office Action at 3).

The rejection is traversed. Jeng `164 does not disclose any of the limitations of the claimed invention. Jeng `164 teaches only a method for increasing the surface area of a stacked capacitor by using an elevated trench isolation structure (Col. 2, lines 19-24). Jeng `164 does not disclose or even mention an isolation trench with two dielectric material areas. The only dielectric material disclosed by Jeng `164 is the TEOS oxide layer 7 which completely fills trench 6. (Col. 3, lines 48-50). Jeng `164 does not disclose "an ion implanted region below" the second area, with substantially all implanted ions being displaced away from separated active regions, as independent claim 68 recites. The only mention to ion implantation in Jeng `164 is the doping of polysilicon via ion implantation, as a well-known method. (Col. 3, lines 25-30). As it is obvious from Figure 12 of Jeng `164, however, the subportions of the p-type substrate 1 under the dielectric layer 12 do not contain implanted ions being displaced away from separated active regions. Further, in Jeng `164, the subportions of the p-type substrate 1 under the dielectric layer 12 are not displaced away from separated active regions by a distance at least equal to a sidewall thickness of said first area," as independent claim 73 recites. Accordingly, the claimed invention is not anticipated by Jeng under § 102.

Similarly, the subportions of the field oxide 14 of Figure 1 of Narita are not part of any isolation trench. In fact, Narita is silent about the existence of an isolation trench in a semiconductor substrate. Further, as illustrated in Figures 1-2, the subportions of the field oxide 14 are in direct contact with gate electrode (word line) 26, and thus not separating active regions, as independent claims 68 and 73 recite. Moreover, Narita does not disclose first and second areas which are respectively filled with a first and second dielectric material, and with substantially all implanted ions displaced away from the separated active regions, as independent claims 68 and 73 recite. Accordingly, the claimed invention cannot be and is not anticipated by Narita under § 102.

Claims 45, 46, 49-52, 54-57, 59, 60, 68-71, and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Kohara et al. (U.S. Patent No. 4, 799, 093) ("Kohara"). The Office Action asserts that the claimed first and second dielectric materials read on subportions of oxide layer 2 of Figure 2C of Kohara and that the claimed ion implanted region reads on region 3 adjacent subportions of region 1. (Office Action at 4).

This rejection is also traversed. Kohara discloses neither areas filled with dielectric materials nor an ion implanted region formed directly below them and as part of a field isolation region, as independent claims 68 and 73 recite. Kohara teaches a method for reducing the surface area of a memory cell by employing a superposed capacitor. (Col. 1, line 68; Col. 2, lines 1-3). In Kohara, the oxide layer 2 of Figure 2C does not comprise a first and second area filled with a first and second dielectric material. In Kohara, the oxide layer 2 is not part of an isolation trench and, thus, the p+ layer 3 cannot be an implanted region formed below an isolation trench, as claims 68 and 73 of the claimed invention recite. Accordingly, none of the limitations of the present invention are described or mentioned in Kohara and, thus, the present invention is not anticipated.

Claims 45, 49-52, and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Kooi et al. (U.S. Patent No. 3, 755, 001) ("Kooi"). The Office Action asserts that the claimed first and second dielectric materials read on subportions of oxide 5 of Figure 8 or oxide 29 of Figure 10 and that the claimed ion implanted region reads on zone 6 of Figure 8 or zone 28 of Figure 10. (Office Action at 4).

The rejection is traversed. Kooi does not disclose an isolation trench or "a second area filled with a second dielectric material" situated within sidewalls of "a first area filled with a first dielectric material," as independent claims 68 recite. Further, Kooi does not disclose "an ion implanted region . . . below said second area," as claim 68 also recites. Kooi is also silent about ion displacement, which is a limitation of claim 68 of "substantially all ions from said ion implanted region being displaced away from said separated active regions." As shown in Figures 8 and 10 of Kooi, the ion implanted regions 6 and 28 are in contact with the dielectric materials 5 and 29, respectively, but these dielectric materials are simply not part of an isolation trench, as independent claim 68 recites. Accordingly, the present invention is not anticipated by Kooi.

Claims 45, 49-52, and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Doo (U.S. Patent No. 3, 386, 865) ("Doo"). The Office Action mentions that, with respect to Figures 5 and 6 of Doo, the claimed first and second dielectric materials read on subportions of oxide 6, and that the claimed ion implanted region comprises region 9. (Office Action at 4).

This rejection is also traversed. Doo teaches a method of making planar semiconductor devices isolated by encapsulating oxide filled channels. (Col. 1, lines 2-4). As such, Doo discloses "isolating channels of the encapsulating SiO_2" below which "p+ regions of semiconductor material" are disposed (Col. 3, lines 68-75), to provide heat dissipation. (Col. 5, line 21). Doo, however, does not disclose a first and second areas

filled with a first and second dielectric material, or "an ion implanted region" with ions which are displaced away from separated active regions," as independent claim 68 recites. In Figures 5 and 6 of Doo, the p+ region 9 is in contact with the SiO_2 filled channel 6, but such SiO_2 filled channel is not part of an isolation trench, as claim 68 recites. Thus, Doo does not anticipate the claimed invention.

Claims 49-52 and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Mastroianni et al. (U.S. Patent No. 4, 443, 932) ("Mastroianni"). The Office Action asserts that the claimed first and second dielectric materials read on subportions of isolation region 125 of Figure 3J and that the claimed ion implanted region reads on a subportion of channel stop region 102 of Figure 3J. (Office Action at 4).

This rejection is also traversed. Figure 3J of Mastroianni does not show or suggest "a second area filled with a second dielectric material" situated within the sidewalls of "a first area filled with a first dielectric material" or "an ion implanted region . . . below said second area," as independent claim 68 recites. Mastroianni is also silent about ion displacement from the separated active regions, as independent claim 68 recites. Again, as in the above-traversed rejections, the channel stop region 102 of Figure 3J of Mastroianni is indeed below the oxide isolation region 125 of the same Figure, but such isolation region is not part of an isolation trench having two areas filled with two dielectric materials. Thus, the claimed invention is not anticipated by Mastroianni.

Claims 45, 49-52, and 68-71 stand rejected under 35 U.S.C. § 102 as being anticipated by Custode et al. (U.S. Patent No. 4, 990, 983) ("Custode"). With reference to Figures 1 and 13 of Custode, the Office Action mentions that the claimed first and second dielectric materials read on the field oxide 34 while the claimed ion implanted region comprises regions 13 and 49. (Office Action at 4).

This rejection is again traversed. Custode discloses a field oxide region under which a heavily doped region is formed to increase threshold voltages. (Col. 1, lines 29-34). As such, a "heavily doped (degenerate) p+ region 13" is formed immediately beneath "thin oxide notched regions 11," which is part of a field oxide 34 (Col. 4, lines 19-23; Figure 13), but which is not part of an isolation trench having two areas filled with two dielectric materials. Custode does not disclose "an ion implanted region . . . below said second area" with "substantially all ions" from the ion implanted region being "displaced away from said separated active regions," as independent claim 68 recites. Further, while the claimed invention is directed to an ion implanted region as part of a field isolation region, the heavily doped (degenerate) p+ region 13 of Custode is not part of a field isolation region. Thus, again, the present invention is not anticipated by Custode.

Finally, claims 45, 46, 49-52, 54-57, 59, 60, 68-71, and 73-75 stand rejected under 35 U.S.C. § 102 as being anticipated by Joo et al. (U.S. Patent No. 5, 841, 163) ("Joo"). The Office Action asserts that the claimed first and second dielectric materials read on the field oxide layer 65 of Figure 15 of Joo, while the claimed ion implanted region comprises layer 68. (Office Action at 5).

This rejection is also traversed. Joo teaches a method for fabricating a memory cell by employing a first and second field insulation layers coupled with a first and second channel stop impurity layers. (Col. 3, lines 38-48). For example, Joo discloses that impurity ions are implanted below the second field oxide layer and are diffused by a thermal process to form a first channel stop impurity layer. (Col. 6, lines 1-3). However, Joo does not disclose first and second areas filled with first and second dielectric materials, or an ion implanted region below the second area, or that substantially all ions in the implanted region are displaced away from the separated active regions, as independent claims 68 and 73 recite. Joo also fails to disclose or suggest the ion spacing limitations recited in claims 68 and 73. Accordingly, the present invention is not anticipated by Joo.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

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